REMARKS

The Examiner is thanked for the thorough review and consideration of the present application. The non-final Office Action dated August 14, 2003 has been received and its contents carefully reviewed.

By this Response, Applicants have amended the specification to correct a minor typographical error, and have amended claims 1, 5 and 8. Claims 1-8 are pending in the application. No new matter has been added. Applicants acknowledge the allowable subject matter of claims 6 and 7, but elect not to rewrite claims 6 and 7 in independent form at this time. Reconsideration and withdrawal of the rejections based upon the above amendments and the following remarks are requested.

In the Office Action, claims 1-4 and 8 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,867,139, issued to Tanaka et al. ("Tanaka"). Applicants traverse the rejection because Tanaka fails to teach or suggest each of the features recited in the claims of the present application. For example, Tanaka fails to teach or suggest a method of driving a liquid crystal display device that includes, among other features, "applying a logic high dummy gate signal to the dummy gate line" as recited in amended independent claim 1; and "generating a plurality of data signals corresponding to a plurality of gate signals, wherein a first one of the data signals corresponds to a first one of the gate signals being an invalid data when the first one of the data signals is in an on position" as recited in amended independent claim 8.

Tanaka discloses an "active matrix type liquid crystal display device that includes scanning lines and signal lines that intersect at right angles". "Scanning signals from a scanning signal drive circuit K are successively applied to the scanning lines 3_1, 3_2,..." (col. 4, lines 59-64), and "a part of the scanning drive circuit K forms signal input means for inputting a signal to the dummy scanning line 3_0" (col. 7, lines 28-30). However, Applicants respectfully submit that Tanaka fails to teach or suggest "applying a logic high dummy gate signal to the dummy gate line" and "generating a plurality of data signals corresponding to a plurality of gate signals, where a first one of the data signals corresponds to a first one of the gate signals being an invalid data when the first one of the data signals is in an open position", as recited in independent claims 1 and 8, respectively.

Because Tanaka fails to teach or suggest each of the features recited in claims 1 and 8, independent claim 1 and its dependent claims 2-4, and independent claim 8 are not anticipated by Tanaka. Reconsideration and withdrawal of the rejection are requested.

In the Office Action, claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Tanaka in view of U.S. Patent No. 5,940,055, issued to Lee. Applicants traverse the rejection because neither Tanaka nor Lee, analyzed along or in any combination, teach or suggest the combined features recited in the claims of the present application. In particular, Tanaka and Lee fail to teach or suggest a driving circuit of a liquid crystal display device that includes, among other features, "a dummy gate driver producing a logic high gate signal of a substantially same waveform as the gate signal, the dummy gate signal being applied to the dummy gate line" as recited in amended claim 5.

The Office Action concedes that Tanaka fails to teach "a dummy gate driver producing a dummy gate signal". To compensate for the deficient teachings of Tanaka, the Office Action relies upon the teachings of Lee. Based upon the teachings of Lee, the Office Action alleges that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the dummy gate driver as taught by Lee in the system of Tanaka in order to provide a driver thereof for preventing non-uniform brightness in the display device independently and efficiently." Applicants disagree.

Lee discloses "LCDs and methods of operating thereof in which the dummy gate line connected to the storage capacitors of a first row of LCD elements of an LCD is driven by a periodic driving voltage which has a magnitude and DC bias sufficient to operate the first row of LCD elements according to a first predetermined transmittance characteristic." (col. 2, lines 24-29) Applicants note that "the gate driver 200 applies gate driving voltages V_{G1}, V_{G2} to a plurality of normal gate lines G_1, G_2 of the LCD panel 100, as well as a periodic driving voltage V_{G0} to a dummy gate line G_0 of the LCD panel 100." (col. 5, lines 14-17 and FIG. 3) As such, Lee fails to teach "a dummy gate driver producing a logic high dummy gate signal of a substantially same waveform as the gate signal, the dummy gate signal being applied to the dummy gate line" as recited in claim 5. Thus, Lee fails to remedy the deficient teachings of

Tanaka, and claim 5 is patentable over Tanaka and Lee. Reconsideration and withdrawal of the rejection are requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue. If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: December 12, 2003

Respectfully submitted,

By Valerie P. Hayes

Valerie P. Hayes
Registration No.: 53,005
MCKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
(202) 496-7500
Attorney for Applicant